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(54) Interconnection structure of a semiconductor device and method of manufacturing the same.

(57) A semiconductor device and a method of manufacturing the same wherein the first and second wirings (12, 14) with an interlayer insulating film (13) interposed therebetween are connected through a contact hole (15) formed in the interlayer insulating film (13). In the semiconductor device, the first and second wirings (12, 14) are connected via a low resistive, conductive metal layer (18) obtained by reducing a highly resistive oxide layer (16) with a highly oxidizing metal (17), the highly resistive oxide layer (16) being exposed within the contact hole (15) on the surface of the first wiring (12). In the method of manufactzuring a semiconductor device, a contact hole (15) is opened in the interlayer insulation (13) on the first wiring (12), a highly oxidizing metal (17) is deposited on the highly resistive oxide layer (16) on the surface of the hirst wiring (12) within the contact hole (15), and the highly resistive oxide layer (16) is reduced with the highly oxidizing metal (17) to change the highly resistive oyide layer to a low resistive, conductive metal layer (18). The second wiring (14) is connected to the first wiring (12) via the conductive metal layer. The reduction may be carried out before or after depositing the second wiring, or at the time when the highly oxidizing metal is deposited.

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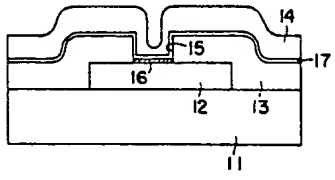

FIG. 1B

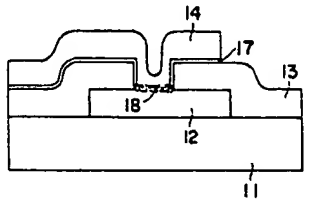

FIG. 1C

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SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

(Field of the Invention)

The present invention relates to a semiconductor device and a method of manufacturing the same and more particularly, to a semiconductor device having a multilayer wiring structure and a method of manufacturing the same.

(Description of the Prior Art)

A conventional multilayer interconnection structure of a semiconductor device will be described with reference to Fig. 3. A first aluminum wiring 2 is formed on a semiconductor substrate 1, and an interlayer insulating film 3 whose main components are silicon oxide film is formed over the aluminum wiring 2. A second aluminum wiring 4 formed on the interlayer insulating film 3 is electrically connected to the first aluminum wiring 2 via a contact hole 5 opened in the insulating interlayer film 3 so as to electrically connect the first aluminum wiring and the second aluminum wiring.

The yield (conduction probability) of conduction decreases rapidly as the diameter of the contact hole 5 becomes very small as shown in Fig. 4. In Fig. 4, line (1) passing through white circles represents the case where the second aluminum wiring is deposited after sputter etching, and line (2) passing through black circles represents the case without sputter etching. As seen from line (2), there scarcely occurs conduction with the contact hole diameter of 1 micron, namely the conduction yield becomes 99.9 % or less. The reason for this is that after the contact hole 5 is formed, the surface of the first aluminum wiring 2 is in contact with air through the contact hole 5 until the second aluminum wiring 4 is formed thereon so that an alumina layer is formed on the surface of the first aluminum wiring 2 to prevent conduction between the first and second aluminum wirings 2 and 4. However, as the diameter of the contact hole 5 becomes large, it is likely for the alumina layer to have some def cts such as pin holes or cracks through which conduction betwe n the first and second aluminum wirings is allowed. In consideration of this, conventionally th alumina lay r on the first aluminum wiring 2 has been removed by sputter etching with Ar ions. Thereafter, while shielding the alumina layer from air, i.e., maintaining in vacuum, the second aluminum wiring 4 is formed on the alumina layer under the same vacuum condition. With the above processes, the conduction yield was made in the order of 99.99 % even with the contact hole diameter of 1 micron as shown in Fig.4, at line (1).

To further improve the yield of conduction, various sputter etching methods are now being developed. Although the conduction yield can be improved by such methods, it has been found that another problem may arise. Namely, where the first aluminum wiring 2 is connected to the gate electrode, a great amount of Ar ions through the sputter etching are implanted in the first aluminum wiring 2 via the contact hole 5 so that the gate oxide film is charged and destroyed. Such damage due to ion implantation becomes more serious as semiconductor devices become finer and the gate oxide film becomes thinner.

As stated above, the conventional method of performing Ar ion sputter etching and removing the alumina layer on the aluminum wiring at the contact hole still poses the problem such as destroying the gate oxide film.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a semiconductor device wherein the alumina layer can be destroyed or removed without damaging the semiconductor device.

According to the semiconductor device of this invention, a highly resistive oxide layer on the surface of the first wiring is reduced with a highly oxidizing metal to form a conductive metal layer through which the first and second wirings are allowed to conduct via a contact hole in the interlayer insulating film. Therefore, the first and second wirings can reliably conduct each other without damage such as the semiconductor being damaged by ion etching.

According to the semiconductor device manufacturing method of this invention, a highly resistive oxide layer formed on the surface of the first wiring and preventing conduction between the first and second wirings, is reduced with a highly oxidizing metal to form a conductive layer. Th refore, th first and second wirings can reliably conduct each other through the conductive metal layer without giving any damage to the semiconductor device.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1C show a first embodiment of the processes of manufacturing a semiconductor device according to the present invention;

Fig. 1D is a sectional view showing a different kind of a semiconductor device manufactured by the method of the first embodiment;

Figs. 2A to 2C show a second embodiment of the processes of manufacturing a semiconductor device according to the present invention;

Fig. 2D is a sectional view showing a different kind of a semiconductor device according to the present invention;

Fig. 3 is a sectional view showing a conventional semiconductor device; and

Fig. 4 is a graph showing the probability of conduction between the first and second wirings.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The first embodiment of the present invention will be described with reference to Figs. 1A to 1C.

As shown in Fig. 1A, a first aluminum wiring 12 is formed on a Si semiconductor substrate 11. An interlayer insulating film 13 whose main component is silicon oxide film is formed over the aluminum wiring 12. A contact hole 15 is formed in the insulating interlayer film 13. An alumina layer 16 in the order of 80 to 100 angstroms in thickness is present on the bottom of the contact hole 15.

Next, as shown in Fig. 1B, a Ti film 17 is deposited on the alumina layer 16 and the interlayer insulating film 13 to a thickness of 500 angstroms by means of a sputter method. A second aluminum wiring 14 is deposited on the Ti film 17 to a thickness of 1 micron by the sputter method similar to the case of the first aluminum wiring 12, without exposing the Ti film 17 to the atmosphere.

Next, a desired wiring pattern is formed by etching the second aluminum wiring 14 and the Ti film 17. Thereafter, the semiconductor device processed as above is subjected to heat treatment in a forming gas composed of N_2 and H_2 at 450 °C for 30 minutes. As a result, as shown in Fig. 1C, an alloy layer 18 is formed at the junction between the first and second wirings 12 and 14. The alloy layer 18 is made of titanium, aluminum and oxygen which are formed through reduction of the alumina layer 16 by the Ti film 17. The alloy layer 18 serves to considerably improve the conduction between the first and second aluminum wirings 12 and 14.

The results of experiments applied to semiconductor devices with the contact hole 15 of 1 micron in diameter showed that the probability of conduction between the first and second wirings 12 and 14 was 99.999 % or more. Checking gate oxide films with 100 angstroms thickness showed that there was no destroyed gate oxide film.

The second embodiment is shown in Figs. 2A to 2C.

The semiconductor device shown in Fig. 2A is similar to that shown in Fig. 1A. A Ti layer 17 and TiN layer 17A are sequentially deposited on the semiconductor device shown in Fig. 2A by means of a sputter method, without exposing both the layers to the atmosphere. Thereafter, a second aluminum wiring 14 is deposited by means of a sputter method.

Next, a desired wiring pattern is formed by etching the second aluminum wiring 14, TiN layer 17A and Ti layer 17. The intermediate stage semiconductor device processed as above is subjected to heat treatment in a forming gas composed of N_2 and H_2 at 450 °C for 30 minutes. As a result, as shown in Fig. 2C, an alloy layer 18A is formed at the junction between the first and second aluminum wirings 12 and 14. The alloy layer 18 is made of titanium, aluminum and oxygen which were formed through reduction of the alumina layer 16 by the Ti film. The alloy layer 18A serves to considerably improve the conduction between the first and second aluminum wirings 12 and 14.

In the second embodiment, the TiN film 17A is not deposited directly on the first aluminum wiring 12, but the Ti film 17 is interposed therebetween. Therefore, it is possible to avoid an increase of contact resistance due to the presence of N_2 at the interface between the first aluminum wiring 12 and the TiN film 17A. Further, since the Ti film 17 is positioned under TiN film 17A, the contact force increases between the TiN film 17A and the insulating interlayer film (SiO_2) 13. Furthermore, since the TiN film 17A is positioned under the second aluminum wiring 14, the resistance against electromigration or thermalmigration is improved. Formation of an alumina layer on the first aluminum wiring 12 may be prevented if an Mo layer is formed on the first aluminum wiring. However, this is not preferable since horizontal hillocks are formed. Also, such a two-layered structure is difficult to etch and likely to produce after-corrosion. The above embodiments are free from such disadvantages.

In the first and second embodiments, the heat treatment is carried out after the second aluminum wiring was deposited. However, the heat treatment may be carried out before the second aluminum wiring 14 is deposited. Alternatively, the heat treatment may be omitted by raising the temperature of the substrate while the Ti film 17 is deposited, and

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enhancing the reaction of the Ti film 17 with the alumina layer 16.

Instead of the Ti film 17 used in the first and second embodiments, highly oxidizing metal such as Hf, V, Mg, Li, Ni or the like and their alloys and the like, such as HfV, AlHf, $NiSi_2$, $HfSi_2$, VSi_2, HfB, VB, HfC, VC, HfN and VN.

Also, instead of aluminum wiring material used in the first and second embodiments, Cu may be used and processed in the similar manner to that for aluminum.

In the first and second embodiments, if the alumina layer 16 is thin and the Ti film 17 is excessive in quantity, the Ti film 17 reacts with Si in the substrate 11 to form alloy spikes which cause leakage in the PN junction. In view of this, a barrier layer 11A (refer to Fig. 1D and Fig. 2D) such as a TiN layer, W layer may be interposed between the first aluminum wiring 12 and the Si substrate 11 to avoid the reaction between aluminum and the Si substrate.

Claims

1. A method of manufacturing a semiconductor device comprising the steps of:
forming an interlayer insulating film (13) on a first wiring (12) :
opening a contact hole (15) in said interlayer insulating film (13) extending to the surface of said first wiring (12);
depositing a highly oxidizing metal (17)within said contact hole (15)where a highly resistive oxide layer (16)is formed on said first wiring;
depositing a second wiring (14) within said contact hole(15)for obtaining conduction between said first and second wirings (12, 14); and
reducing said highly resistive oxide layer (16) with said highly oxidizing metal (17) to change said highly resistive oxide layer(16)to a low resistive, conductive metal layer (18)by means of heat treatment, said reduction step being performed at any time after said contact hole opening step.

2. A method of manufacturing a semiconductor device according to claim 1, wherein said reduction step is performed after said second wiring deposition step.

3. A method of manufacturing a semiconductor device according to claim 1, wherein said reduction step is performed after said highly oxidizing metal deposition step and before said second wiring deposition step.

4. A method of manufacturing a semiconductor device according to claim 1, wher in said reduction step is performed at the time when said highly oxidizing metal deposition step is performed.

5. A method of manufacturing a semiconductor device according to claim 1, wherein the mat rial of said first and second wirings (12, 14) is selected from the group consisting of Al and Cu.

6. A method of manufacturing a semiconductor device according to claim 1, wherein said highly oxidizing metal (17)is selected from the group consisting of Ti, V, Mg, Li, Ni, HfV, AlHf, $NiSi_2$, $HfSi_2$, VSi_2, HfB, VB, HfC, VC, HfN and VN.

7. A method of manufacturing a semiconductor device according to claim 1, wherein said reduction step is performed by heat treatment in a forming gas made of N_2 and H_2.

8. A method of manufacturing a semiconductor device according to claim 1, wherein said highly oxidizing metal(17)is Ti which is deposited to the thickness of 500 angstroms, and said first and second wirings (12, 14)are Al, the second wiring (14) Al being deposited to the thickness of 1 micron.

9. A semiconductor device comprising:
a first wiring (12)
an interlayer insulating film (13) formed on said first wiring (12) and having a contact hole (15) extending to the surface of said first wiring (12);
a low resistive, conductive metal layer (18) obtained by reducing a highly resistive oxide layer (16) with a highly oxidizing metal, said highly resistive oxide layer (16) being exposed within said contact hole (15) on the surface of said first wiring (12); and
a second wiring (14) which conducts with said first wiring (12)via said conductive metal layer (18)

10. A semiconductor device according to claim 9, wherein the material of said first and second wirings (12, 14)is selected from the group consisting of Al and Cu.

11. A semiconductor device according to claim 9, wherein said highly oxidizing metal(17)is selected from the group consisting of Ti, V, Mg, Li, Ni, HfV, AlHf, $NiSi_2$, $HfSi_2$, VSi_2, HfB, VB, HfC, VC, HfN and VN.

12. A semiconductor device according to claim 9, wherein said highly oxidizing metal (17) which is deposited to the thickness of 500 angstroms is Ti, and said first and second wiring materials (12, 14)-are Al, the second wiring (14) Al being deposited to the thickness of 1 micron.

13. A semiconductor device according to claim 9, wherein said first wiring (12) is formed on a Si semiconductor substrate (11) with a barrier layer (11A) such as TiN layer or W layer interposed therebetween.

14. A semiconductor device according to claim 9, wherein said second wiring (14) is formed on said interlayer insulating film (13), with said highly

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oxidizing metal (17)and a barrier layer (17A)such as TiN layer or W layer interposed therebetween.

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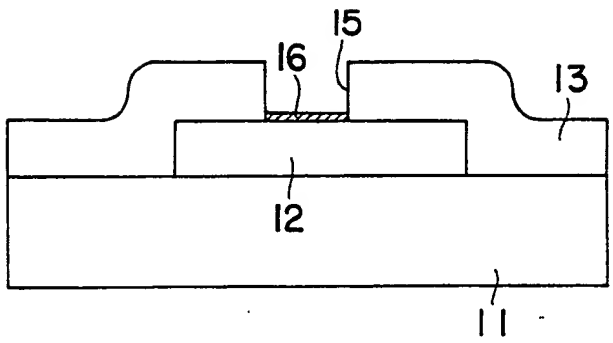


FIG. 1A

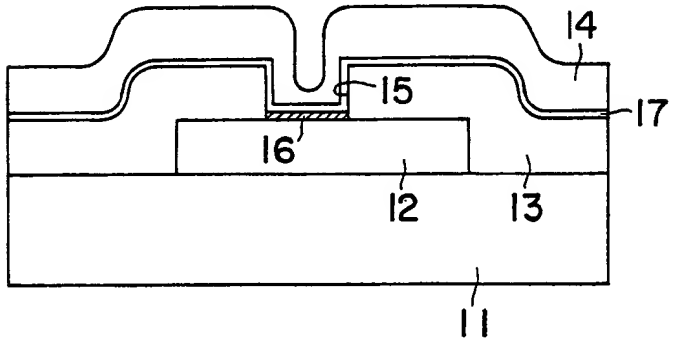


FIG. 1B

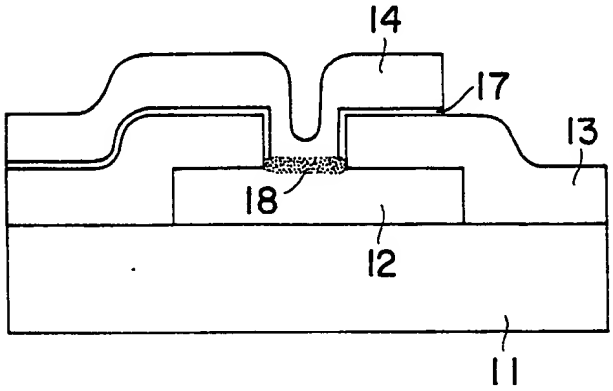


FIG. 1C

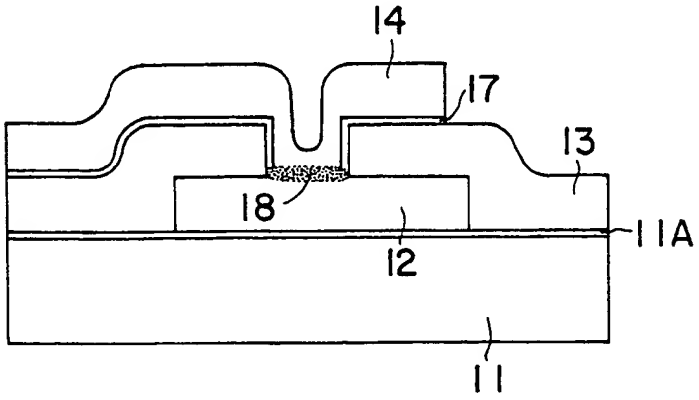


FIG. 1D

FIG. 2A

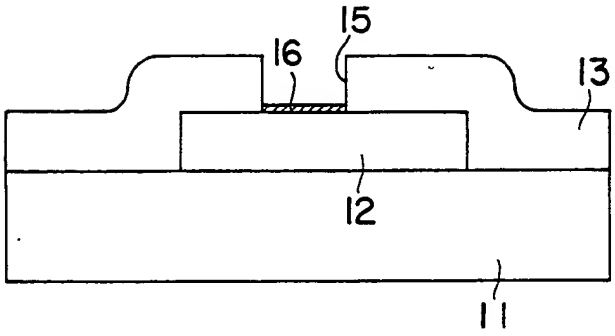


FIG. 2B

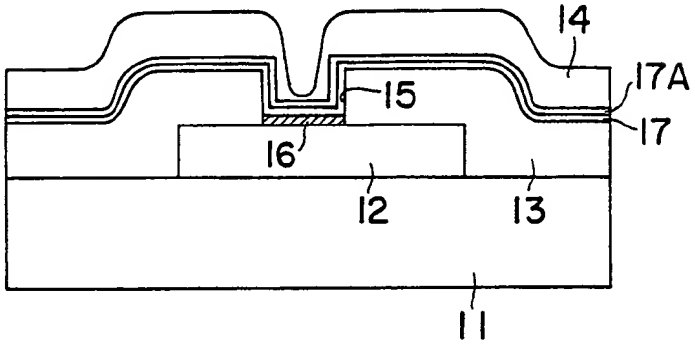


FIG. 2C

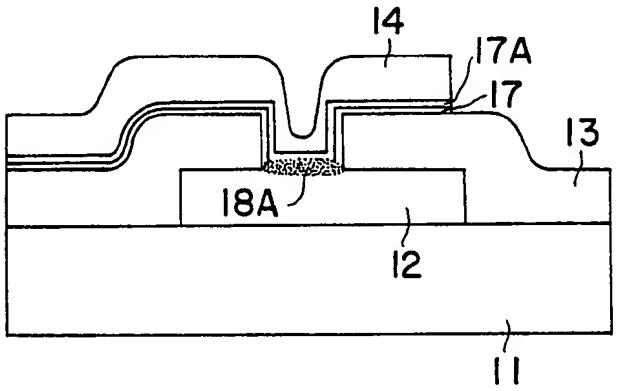
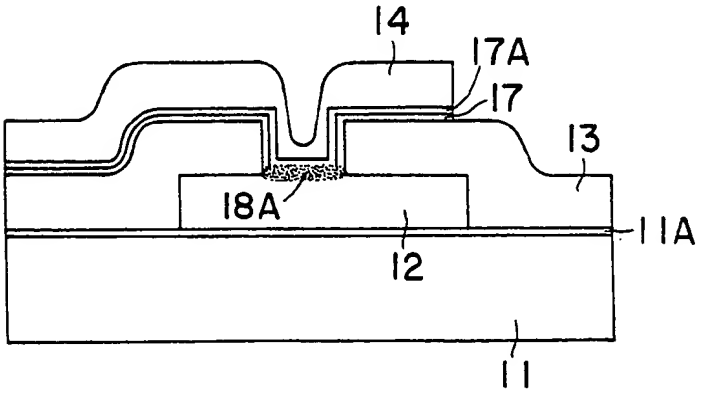


FIG. 2D



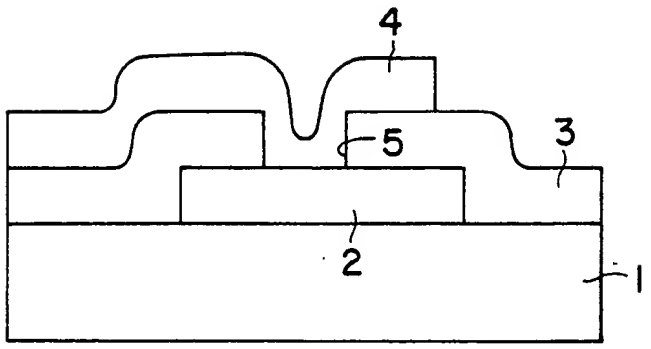


FIG. 3 PRIOR ART

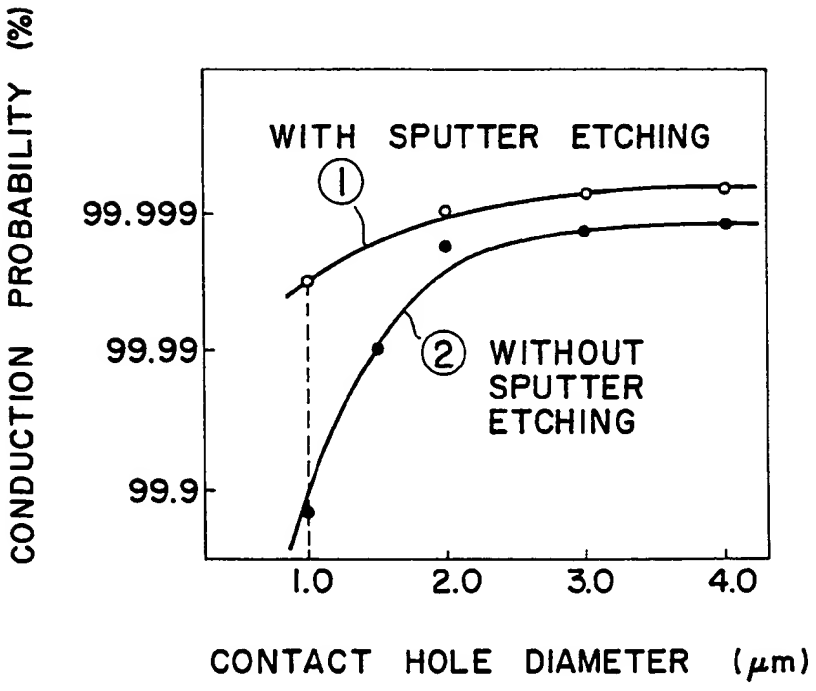


FIG. 4 PRIOR ART

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06.02.91 Bulletin 91/06

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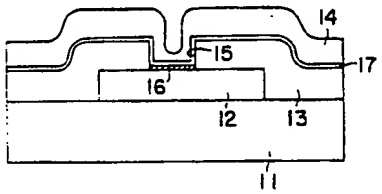

FIG. 1B

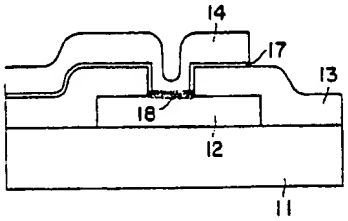

FIG. 1C

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 88 11 6171

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	EP-A-0 042 926 (ROCKWELL INTERNATIONAL) * the whole document *	1,2,5-7, 9-11	H 01 L 21/90 H 01 L 21/74
X	DE-A-3 414 781 (MITSUBISHI DENKI) * page 6, lines 10-18; page 7, lines 11-14; page 8, lines 12-15; page 10, line 17 - page 11, line 33 *	1,2,5,6, 8-12	
Y		13,14	
Y	PROCEEDINGS OF THE FOURTH INTERNATIONAL IEEE VLSI MULTILEVEL INTERCONNECTION CONFERENCE 15,16 June 1987, pages 148-154, Santa Clara, CA, US; S. MURAKAMI et al.:"Plasma-Nitridated Ti Contact System for VLSI Interconnections" * figure 1; pages 148,149 *	13,14	
A	US-A-4 507 852 (P.C. KARULKAR) * figure 2a; abstract; claims *	8,12	
A	GB-A-2 135 123 (RCA) * page 1, lines 26-52; figures *	1,9	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)
H 01 L

The present search report has been drawn up for all claims

Place of search	Date of completion of search	Examiner
Berlin	05 November 90	JUHL A.

CATEGORY OF CITED DOCUMENTS

X: particularly relevant if taken alone
Y: particularly relevant if combined with another document of the same catagory
A: technological background
O: non-written disclosure
P: intermediate document
T: theory or principle underlying the invention

E: earlier patent document, but published on, or after the filing date
D: document cited in the application
L: document cited for other reasons

&: member of the same patent family, corresponding document